AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor package comprising:

a plurality of leads, each of the leads defining first and second surfaces and including:

a pad portion; and

at least one connecting bar portion integrally connected to and extending from the pad portion;

at least some of the leads each having a bump land formed on the second surface upon the pad portion thereof and at least some of the leads each having a bump land formed on the second surface upon the connecting bar portion thereof,

the pad portions of the leads being segregated into an outer set and an inner set, with the pad portions of the inner set each including a bump land formed thereon and the at least one connecting bar portion extending from each of the pad portions of the outer set defining an inner end having a bump land formed thereon, the inner ends of at least some of the connecting bar portions being positioned within an internal region defined by the inner set of pad portions;

a semiconductor chip defining opposed first and second surfaces and including a plurality of input/output pads disposed on the first surface thereof;

a plurality of conductive bumps electrically connecting the input/output pads to respective ones of the bump lands; and

an encapsulant portion covering the semiconductor chip, the conductive bumps, and the second surfaces of the leads such that at least portions of the first surfaces of the leads are exposed within the encapsulant portion.

2. (Original) The semiconductor package of Claim 1 wherein the first surface of the semiconductor chip is disposed at a prescribed separation distance from the second surfaces of the leads.

3. (Original) The semiconductor package of Claim 1 wherein:

the first and second surfaces of each of the leads are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surfaces thereof;

the third surface of each of the leads is covered by the encapsulant portion; and

the first surface of each of the leads is exposed within the encapsulant portion to serve as an input/output terminal.

4. (Cancelled)

5. (Previously Amended) The semiconductor package of Claim 1 wherein each of the leads includes a protective layer formed on the second surface thereof other than for a prescribed region defining the bump land.

6. (Original) The semiconductor package of Claim 5 wherein the protective layer is selected from the group consisting of:

a polyimide;

titanium; and

aluminum.

7. (Cancelled)

8. (Cancelled)

9. (Currently Amended) The semiconductor package of Claim **[[8]]** **1** wherein:

the first and second surfaces of each of the leads are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surfaces thereof in opposed relation to that segment of the second surface which extends along the connecting bar portion;

the third surface of each of the leads is covered by the encapsulant portion; and

the first surface of each of the leads extending along the pad portion thereof is exposed within the encapsulant portion to serve as an input/output terminal.

10. (Currently Amended) A semiconductor package comprising:

a plurality of leads, each of leads defining first and second surfaces and including:

a pad portion;

at least one connecting bar portion integrally connected to and extending from the pad portion;

a protective layer formed on the second surface; and

a bump land formed on the second surface and at least partially circumvented by the protective layer;

at least some of leads each having the bump land formed on the pad portion thereof and at least some of the leads each having the bump land formed on the connecting bar portion thereof,

the pad portions of the leads being segregated into an outer set and an inner set, with the pad portions of the inner set each including a bump land formed thereon and the at least one connecting bar portion extending from each of the pad portions of the outer set defining an inner end having a bump land formed thereon, the inner ends of at least some of the connecting bar portions being positioned within an internal region defined by the inner set of pad portions;

a semiconductor chip having a plurality of input/output pads disposed thereon;

a plurality of conductive bumps electrically connecting the input/output pads to respective ones of the bump lands; and

an encapsulant portion covering the semiconductor chip, the conductive bumps, and the leads such that at least a portion of the first surface of each of the leads is exposed in the encapsulant portion;

11. (Previously Presented) The semiconductor package of Claim 10 wherein the semiconductor chip has a first surface which is disposed at a prescribed separation distance from the second surfaces of the leads.

12. (Previously Presented) The semiconductor package of Claim 10 wherein:

the first and second surfaces of each of the leads are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surfaces thereof; and

the third surface of each of the leads is covered by the encapsulant portion.

13. (Previously Presented) The semiconductor package of Claim 10 wherein the protective layer comprises one of polyimide, titanium and aluminum.

14. (Canceled)

15. (Previously Presented) The semiconductor package of Claim 10 wherein:

the first and second surfaces of each of the leads are generally planar and extend in opposed relation to each other;

each of the leads further includes a third surface formed between the first and second surfaces thereof in opposed relation to a segment of the second surface which extends along the connecting bar portion;

the third surface of each of the leads is covered by the encapsulant portion; and

the first surface of each of the leads extending along the pad portion thereof is exposed in the encapsulant portion.

16. (Previously Presented) The semiconductor package of Claim 10 wherein the pad portions and the bump lands each have a circular footprint.

17. (New) The semiconductor package of Claim 1 wherein the plurality of input/output pads disposed on the first surface of the semiconductor chip are positioned directly above the bump lands formed on the pad portions of the inner set and the bump lands formed on the inner ends of the connecting bars positioned within the internal region.

18. (New) The semiconductor package of Claim 1 wherein all of the inners ends of the connecting bar portions are positioned within the internal region.

19. (New) The semiconductor package of Claim 10 wherein the plurality of input/output pads disposed on the semiconductor chip are positioned directly above the bump lands formed on the pad portions of the inner set and the bump lands formed on the inner ends of the connecting bars positioned within the internal region.

20. (New) The semiconductor package of Claim 10 wherein all of the inners ends of the connecting bar portions are positioned within the internal region.